

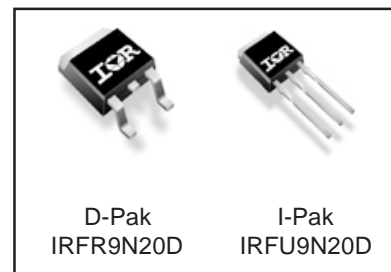
**Applications**

- High frequency DC-DC converters

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
<b>200V</b>	<b>0.38Ω</b>	<b>9.4A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.4	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6.7	
$I_{DM}$	Pulsed Drain Current ①	38	
$P_D @ T_C = 25^\circ C$	Power Dissipation	86	W
	Linear Derating Factor	0.57	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Typical SMPS Topologies**

- Telecom 48V input Forward Converter

Notes ① through ⑥ are on page 10

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# IRFR9N20D/IRFU9N20D

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Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.38	$\Omega$	$V_{GS} = 10V, I_D = 5.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	4.3	—	—	S	$V_{DS} = 50V, I_D = 5.6A$
$Q_g$	Total Gate Charge	—	18	27	nC	$I_D = 5.6A$ $V_{DS} = 160V$ $V_{GS} = 10V, \text{④}$
$Q_{gs}$	Gate-to-Source Charge	—	4.7	7.1		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	9.0	14		
$t_{d(on)}$	Turn-On Delay Time	—	7.5	—	ns	$V_{DD} = 100V$ $I_D = 5.6A$ $R_G = 11\Omega$ $V_{GS} = 10V, \text{④}$
$t_r$	Rise Time	—	16	—		
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		
$t_f$	Fall Time	—	9.3	—		
$C_{iss}$	Input Capacitance	—	560	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V \text{ ⑤}$
$C_{oss}$	Output Capacitance	—	97	—		
$C_{rss}$	Reverse Transfer Capacitance	—	29	—		
$C_{oss}$	Output Capacitance	—	670	—		
$C_{oss}$	Output Capacitance	—	40	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	74	—		

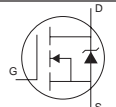
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	100	mJ
$I_{AR}$	Avalanche Current①	—	5.6	A
$E_{AR}$	Repetitive Avalanche Energy①	—	8.6	mJ

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	9.4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	38		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 5.6A, V_{GS} = 0V, \text{④}$
$t_{rr}$	Reverse Recovery Time	—	130	—	ns	$T_J = 25^\circ\text{C}, I_F = 5.6A$
$Q_{rr}$	Reverse Recovery Charge	—	560	—	nC	$di/dt = 100A/\mu s, \text{④}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

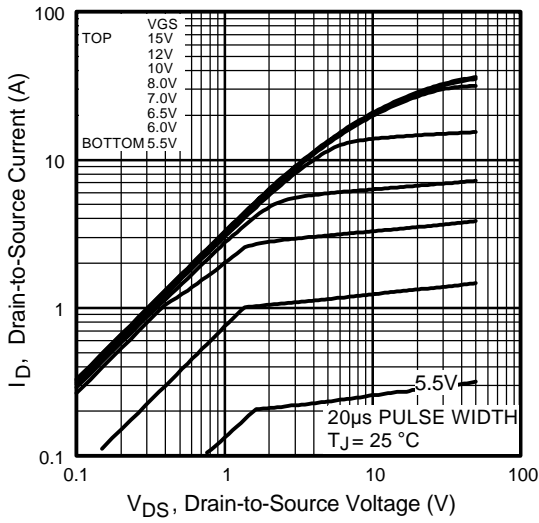


Fig 1. Typical Output Characteristics

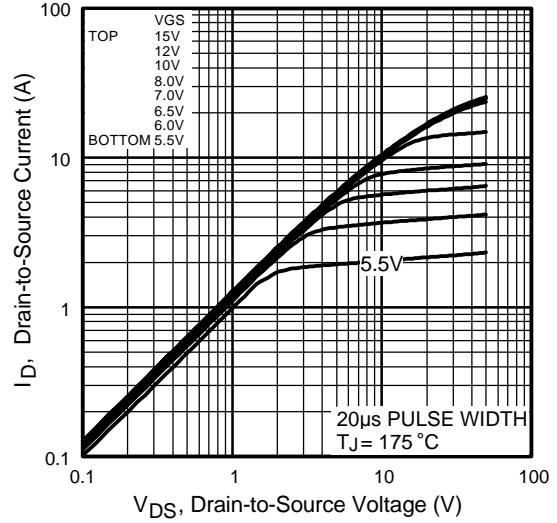


Fig 2. Typical Output Characteristics

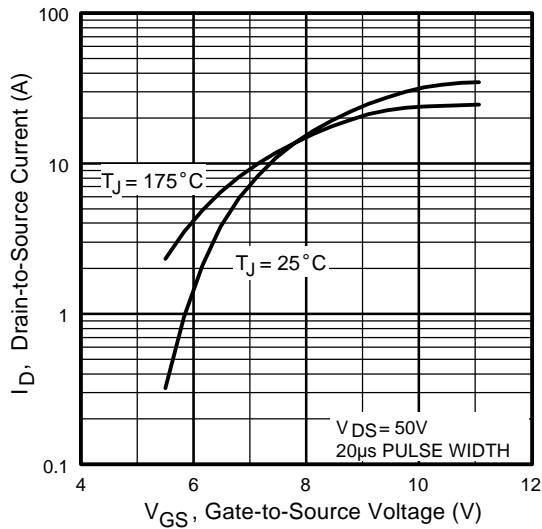


Fig 3. Typical Transfer Characteristics

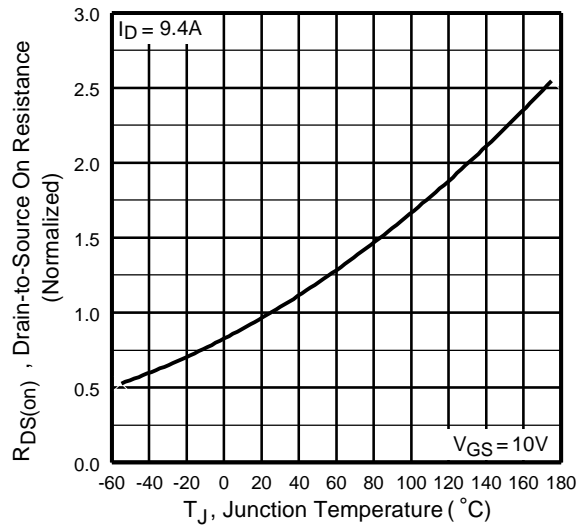
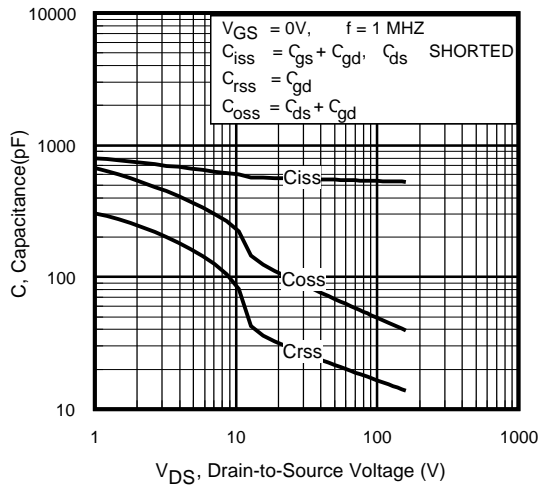


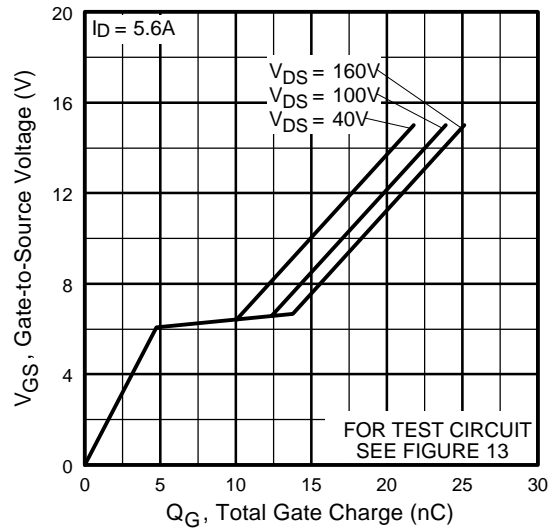
Fig 4. Normalized On-Resistance Vs. Temperature

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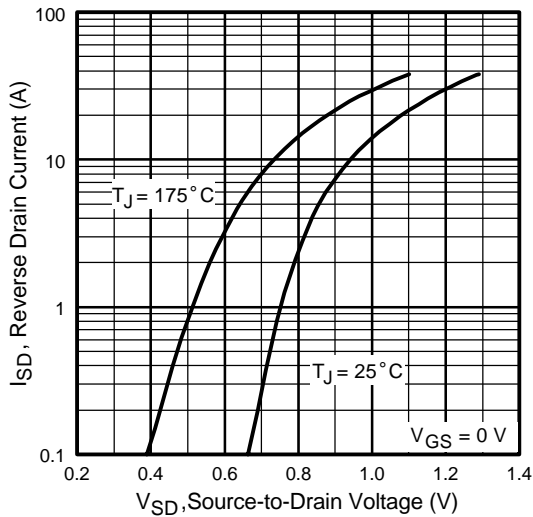
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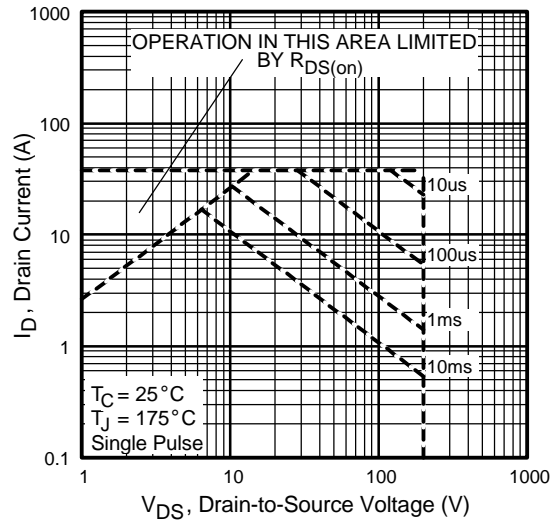
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



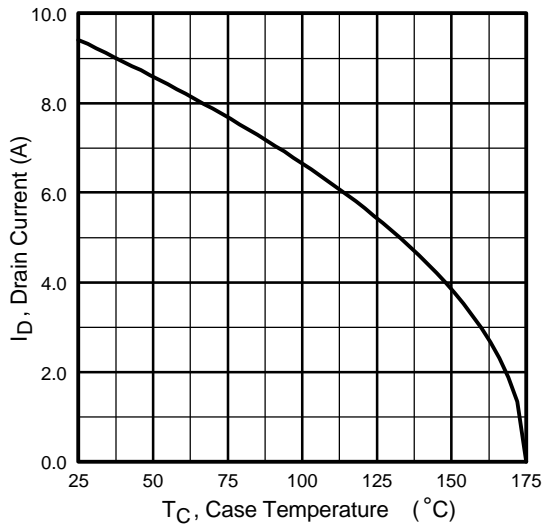
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



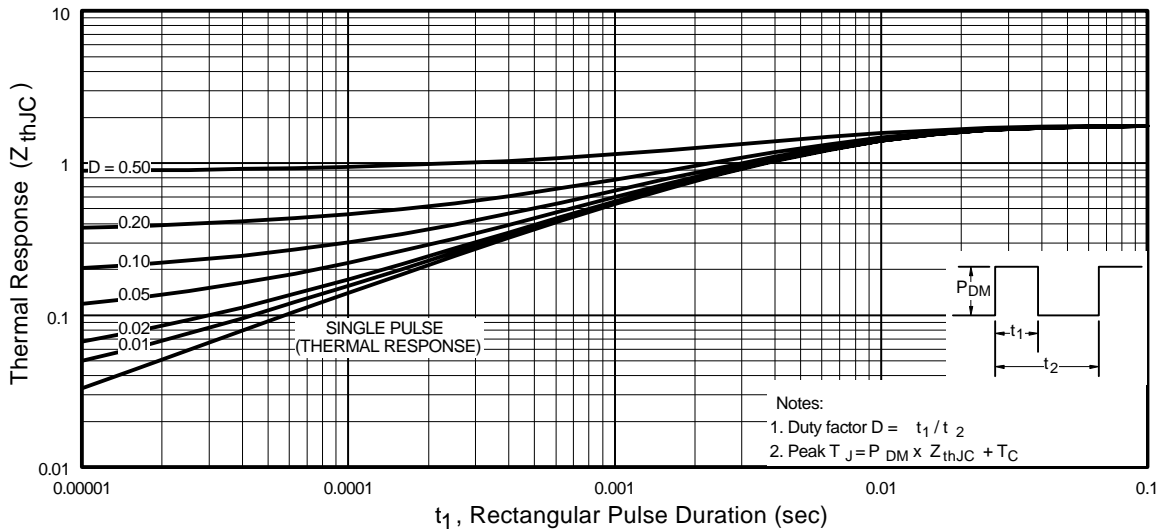
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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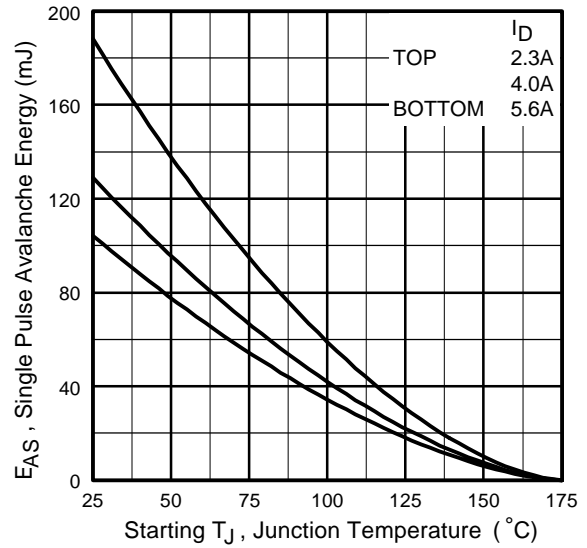
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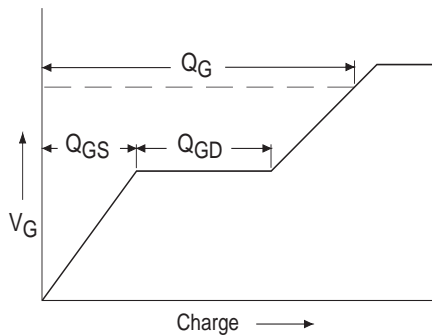
**Fig 12a.** Unclamped Inductive Test Circuit



**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

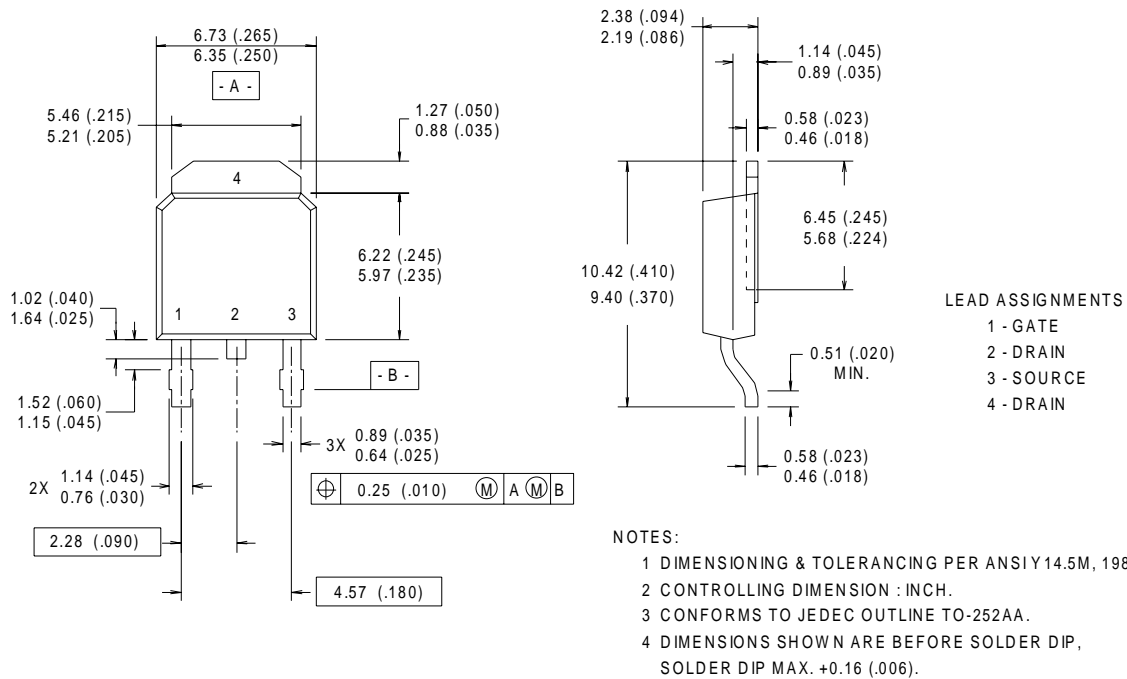
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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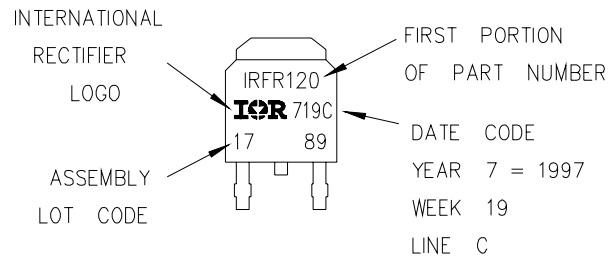
## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



## D-Pak (TO-252AA) Part Marking Information

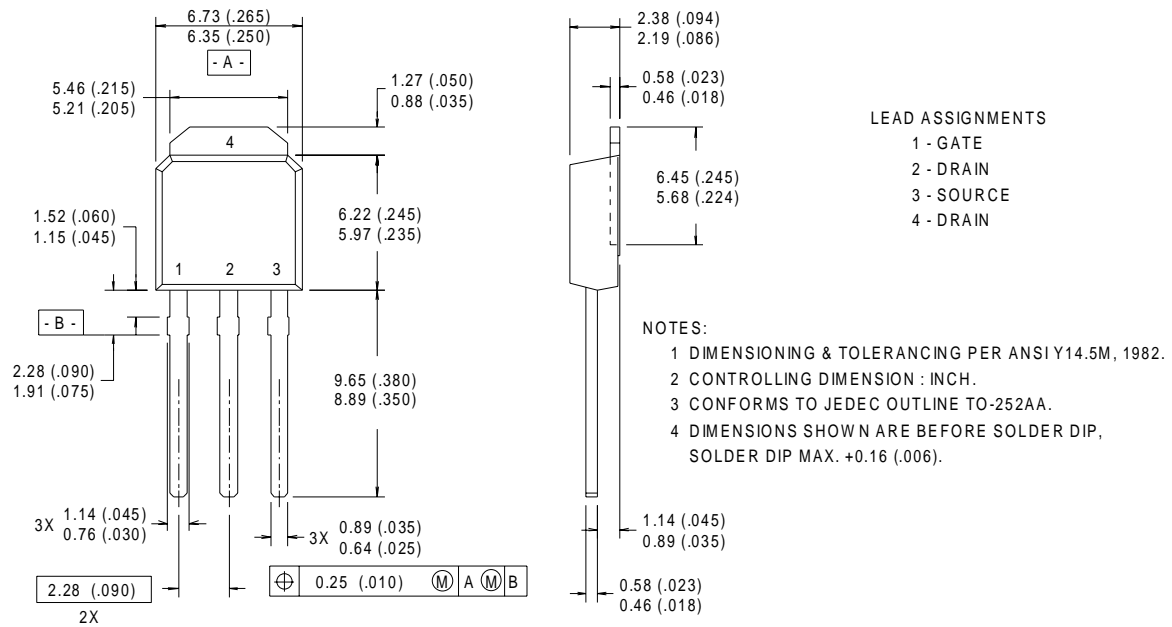
EXAMPLE: THIS IS AN IRFR120  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

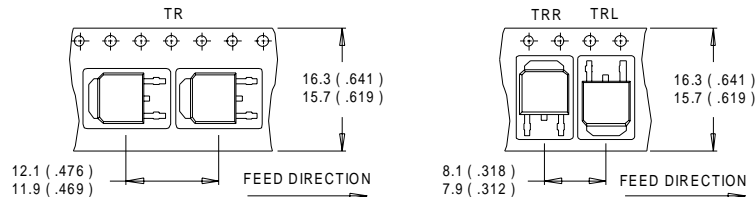


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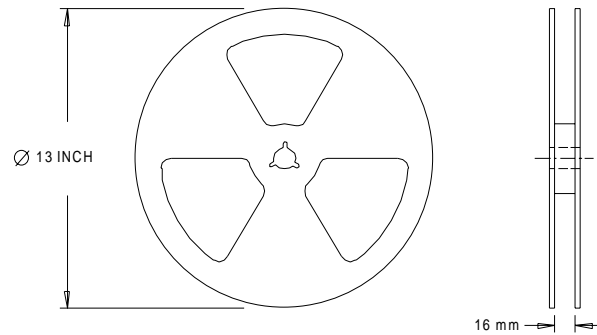
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## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 6.4\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 5.6\text{A}$ .
- ③  $I_{SD} \leq 5.6\text{A}$ ,  $di/dt \leq 110\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

\* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

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*Data and specifications subject to change without notice. 6/00*